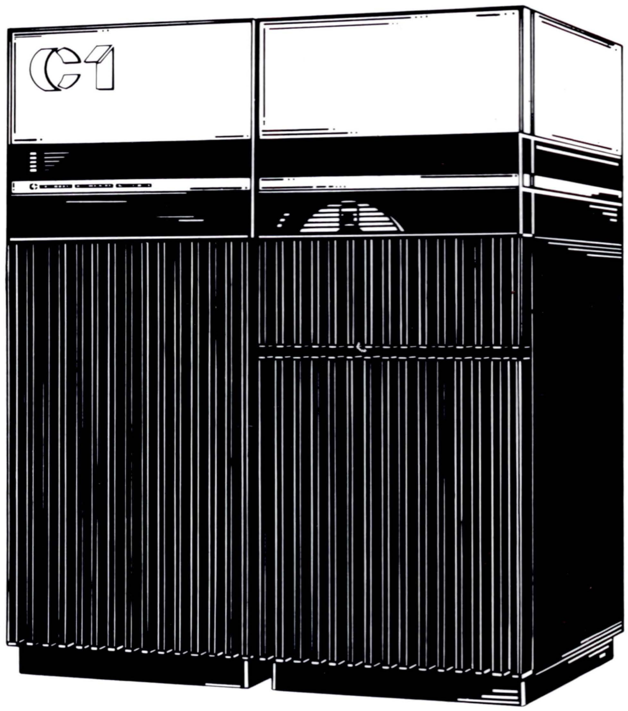
CONVEX

C-1 COMPUTER SYSTEM



The CONVEX C-1™ 64-bit supercomputer system sets a new standard for price/performance in scientific computing applications. By using a combination of widely accepted software and hardware standards, implemented with advanced technology, the CONVEX C-1 system offers the scientific user access to supercomputer performance at minicomputer prices.

A well-balanced computer system, the CONVEX C-1 computer blends high-speed 64-bit integrated scalar and vector processing with large real and virtual memory, high-performance input/output, and productivity-oriented system software.

FEATURES

High-performance supercomputer system

- High-speed 64-bit scientific computer with integrated scalar and vector processing
- 4 Gigabytes of virtual address space
- Main memory expansion to 16 Mwords (128 MBytes)
- Multiple, high-performance cache memories
- RISC (Reduced Instruction Set Computer) architecture
- Highly-pipelined implementation
- Independent, high-performance intelligent I/O subsystems
- High-performance I/O bus with 80 MBytes per second bandwidth
- Extensive reliability, availability, and serviceability features
- Extensive use of high density CMOS VLSI gate arrays for low power and high reliability
- Compact package, 5 feet high, 19-inch RETMA rack
- Rugged construction and low power consumption

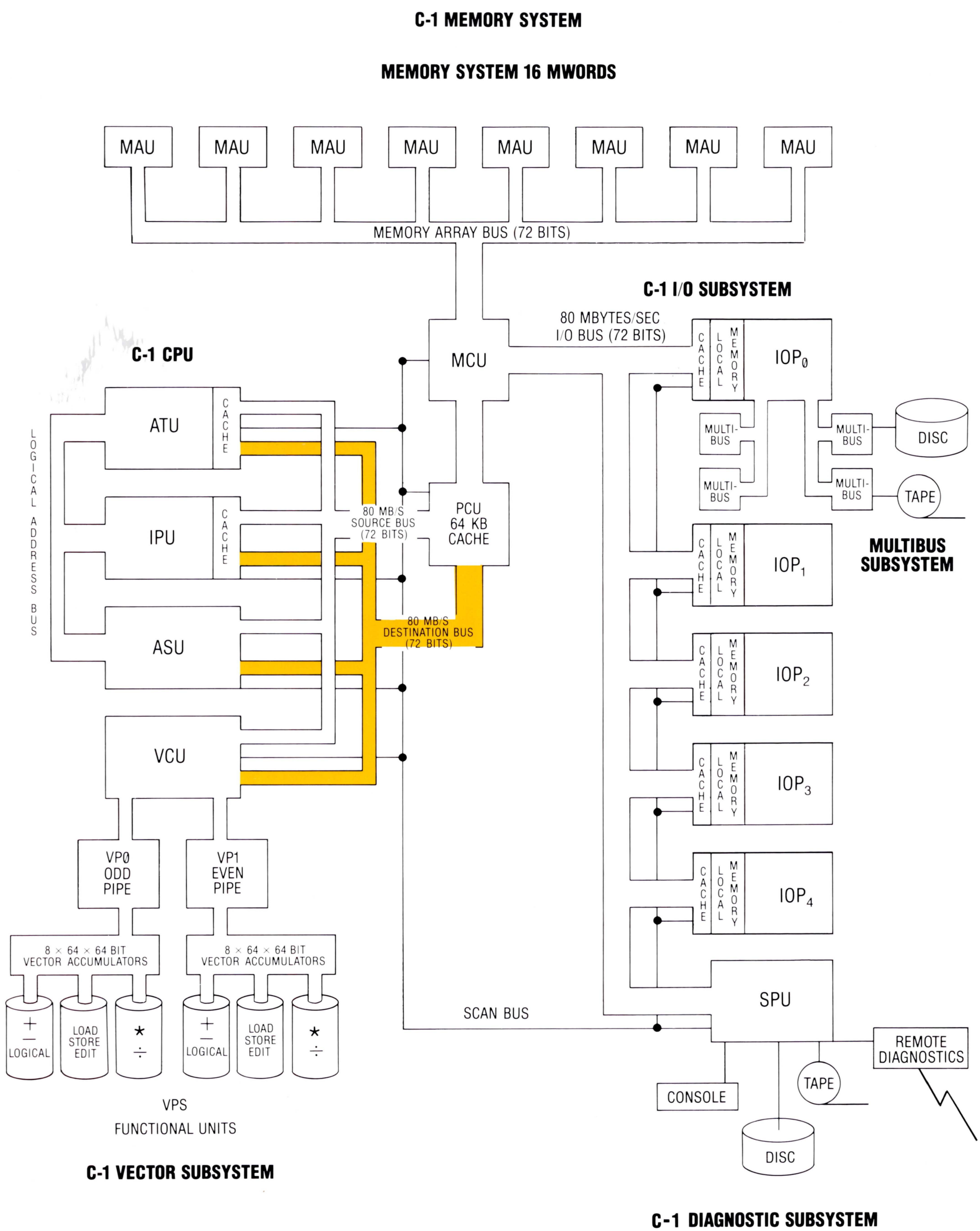


Figure 1. C-1 Supercomputer Block Diagram

HIGH PERFORMANCE I/O

The CONVEX C-1 Input/Output system possesses both a highly intelligent I/O processing system and high-throughput Input/Output bus. The CONVEX C-1 supports up to five Input/Output Processors (IOP's). Each IOP is an autonomous processor based on a 10 MHz 32-bit processor with local memory.

CONVEX UNIX takes full advantage of this underlying architecture with the kernel distributed between the CPU and the IOP's. Each IOP contains an executive and the peripheral device drivers that control and manage all peripheral device functions: addressing; interrupt handling; data transfers, and so on. In other words, the CPU is not impeded handling mundane I/O functions.

An IOP has two external interfaces. One interface is to the CONVEX 80 MBytes/second I/O bus. The other interface is to two buses that connect to multiple MULTIBUS card cages.

Each IOP, via these connections, can support up to 4 MULTIBUS card cages. Each card cage may contain up to 8 controllers, for a total of 160 device controllers in the system. Aiding in the interface between the IOP's and the MULTIBUS™ is a data cache in the IOP. This 32 KBYTE cache performs the necessary buffering between the slower MULTIBUS and the high-speed CONVEX I/O bus.

As a result of using the industry-standard MULTIBUS, the CONVEX C-1 supports a wealth of peripheral devices, including disk drives, tape drives, printers, alphanumeric terminals, and communications interfaces.

RELIABILITY/AVAILABILITY/ SERVICE

Central to the overall design philosophy of the CONVEX C-1 is a well-thought out and implemented reliability/availability/service system. Integral to the CONVEX C-1 is a Service Processor Unit (SPU). The SPU is a microprocessor-based unit that controls the operation of diagnostic programs and maintains a log of detected and corrected errors. The SPU runs under its own diagnostic UNIX operating system, and contains a 17.5 MByte Winchester disk and cartridge tape as peripheral devices, as well as communications ports for the operator's console and for remote diagnostics. The disk maintains an on-line log of errors as well as code for the diagnostics. The cartridge tape, with a formatted capacity of 25 MBytes, is used for software distribution for both system and diagnostic software and may be used as a distribution medium for user software.

This very flexible and powerful SPU system controls one of the most sophisticated diagnostic systems available. Each subsystem is interfaced to the SPU via a proprietary diagnostic scan bus. Once initiated, the diagnostic system scans-in test patterns and scans-out results, without using any of the buses used during normal computations. This approach results in high resolution diagnostics, thereby significantly reducing the mean time to repair. In addition, the provision of a remote diagnostics capability improves the efficiency of maintenance personnel and results in minimum downtime.

Additional advanced features include: extensive parity checking throughout the entire design; single-bit error correction and double-bit error detection for main memory accesses, and alterable control store within the ASU and VPS. Diagnostic-readable serial numbers are contained on each logic board; this feature permits the diagnostic system to ensure that boards are up to the latest revision level and in the proper slots.

COMPACT, RUGGED PACKAGING

The CONVEX C-1 system is housed in a standard 19 inch RETMA rack, and stands 5 feet high. Contained within this rack are: the CONVEX C-1 central processing unit; up to 16 MWords of main memory; up to 5 IOP's; the SPU with its floppy tape and Winchester disk, and one MULTIBUS card cage. The minimum system configuration includes a second, adjacent rack, which contains a 6250 bpi tape drive and one 414MB formatted Winchester disk drive—resulting in an extremely powerful system in a compact package.

The CONVEX C-1 is air cooled, with cooling provided by two fans drawing air through the front of the rack and exhausting through the rear.

All CONVEX processor boards are vertically mounted and attached to the backpanel via rugged 96-pin DIN connectors. To ensure rigidity, these boards are fastened to the card cage with a screw-type ejector and injector mechanism.

The components packaged in the processor cabinet consume approximately 3200 watts of input power in the standard configuration, and less than 4500 watts when fully configured with 16 MWords of main memory and 5 IOP's. The system operates in a temperature range between +15 and +32 degrees centigrade.

VIRTUAL MEMORY OPERATING SYSTEM—UNIX (4.2 bsd)

The CONVEX operating system is derived from the Berkeley 4.2 UNIX™ operating system. The CONVEX architecture is designed to support CONVEX UNIX efficiently. The architecture directly supports a 4096 byte page size, hardware referenced and modified bits, and a hierarchical protection system based on a ring structure. These hardware features, coupled with the advanced features of UNIX, provide the user with a highly-productive development environment as well as a production system for applications needing certain real-time capabilities. Among the standard features supported are:

- System virtual address space of 4 Gigabytes
- User virtual address space of 2 Gigabytes.
- Multi-user development environment
- Interprocess communications
- Process priority levels
- Interactive user interfaces through the C and Bourne shells
- Hierarchical file system

PROGRAMMING LANGUAGES

Initially, two high-level languages are provided: C and FORTRAN. The C language is compatible with the C compiler which comes with the standard UNIX distribution.

The FORTRAN compiler is ANSI standard FORTRAN '77 with extensions conforming to those found in the VAX/VMS™ FORTRAN Compiler and support for certain FORTRAN '66 features. The data type extensions include support for *1, *2, *4, and *8 integers and logical operands. Also, there is support for REAL *4 and REAL *8 as well as COMPLEX *8 and *16.

The CONVEX FORTRAN compiler performs sophisticated optimizations and vectorizations. The scalar optimizations performed include: global constant propagation and folding, global common sub-expression elimination, global strength reduction, code motion optimizations and dead code removal. After these optimizations are applied, vectorization is performed.

Vectorization is a process by which the FORTRAN compiler translates an iterative sequential procedure into parallel execution. The aim of this process is to utilize the architectural capabilities of the CONVEX hardware to produce optimal executable code, while the programmer writes in standard FORTRAN.

DEVELOPMENT TOOLS

CONVEX provides a broad family of tools to maximize the productivity of programmers. These utilities, coupled with a hierarchical file system, RISC architecture, and multiple IOP's, result in a highly-productive programming environment as well as extremely high performance.

PERIPHERAL PRODUCTS

CONVEX offers a variety of high-performance peripheral products to fulfill the requirements of the scientific user. These include:

- Disk Drives
  - — 414 Megabyte (formatted) Winchester drive
- Magnetic Tape Units
  - — High-Performance: 6250/1600/800 bpi, 125 ips
  - — Medium-Performance: 6250/1600 bpi, 50 ips
- Line Printer/Plotter: 600 Lines per minute
- Video Terminal: VT-100 Compatible
- Communications Multiplexer: 16 asynchronous lines (Supports RS232)

Comprehensive system software

- CONVEX UNIX™ virtual memory operating system derived from 4.2 bsd, with real-time and batch queue extensions
- Globally optimizing and vectorizing ANSI FORTRAN '77 compiler
- C Compiler and native assembly language
- Over 200 utilities for editing, debugging, source code maintenance, macro processing, and program performance analysis

Extensive user and program capacity.

- Fast, consistent response in multi-user timesharing environment
- User program size up to 2 gigabytes
- 5-level address space protection
- Intelligent Input/Output Processors (IOP's) for concurrent I/O control.
  - — MULTIBUS™ subsystem for connection of up to 160 peripheral devices.

HIGH-PERFORMANCE COMPUTER WITH INTEGRATED VECTOR PROCESSING

The CONVEX C-1 supercomputer is a high performance system based on a proprietary, bus-oriented architecture. The central processing unit (CPU) portion of the system utilizes a CRAY™-like architecture. This architecture employs 64-bit integrated scalar and vector processing and multiple arithmetic units to achieve peak processing rates exceeding 60 million computations per second.

The C-1 central processor consists of multiple asynchronous units, operating concurrently in a pipelined fashion. These units are interconnected through multiple high-speed 64-bit buses. The asynchronous nature of these units permits up to 8 operations to be executing at the same time. The inclusion of a highly-intelligent I/O system permits the vast majority of I/O operations to be concurrently executed and controlled independent of the central processor. The off-loading of these functions makes the central processor much more productive. (See Figure 1.)

The central processor consists of the following subsystems:

INSTRUCTION PROCESSING UNIT (IPU)

The Instruction Processing Unit fetches and decodes instructions. To accelerate these functions the IPU contains a 1024-byte logical instruction cache. This instruction cache, coupled with a unique decoding mechanism, permits conditional and unconditional branches to be executed entirely within the IPU and in parallel with the operation of other units within the central processor. Instructions are decoded every 100 nanoseconds. This decoding mechanism, along with the use of multiple program counters, results in a conditional branch being executed in one 100-nanosecond cycle.

ADDRESS AND SCALAR UNIT (ASU)

For those instructions that require the generation of logical addresses or the manipulation of scalar data, a dedicated address and scalar unit is provided. The ASU is an autonomous subsystem that is controlled by a 4096-word RAM-based control store. It is capable of generating logical addresses or performing scalar operations every 100 nanoseconds. The ASU contains a unique hazard detection and control mechanism that permits multiple scalar operations to be executed concurrently.

ADDRESS TRANSLATION UNIT (ATU)

Logical addresses must be translated to physical addresses before referencing main memory. The address translation unit provides this function as well as several acceleration mechanisms. The ATU contains a logical cache, which holds the most frequently referenced data operands. This unique cache associates on logical addresses as contrasted with the more conventional physical address association. The result is high performance accessing of operands, especially as they relate to subroutine entry, exit, and argument usage. The ATU also contains an address cache. Once a logical address is translated, the translated address is maintained in a 1024-entry address cache. As with the IPU and ASU, the ATU operates in a 100-nanosecond pipelined fashion.

Data in the CONVEX machine is byte-addressable. Thus scalar and vector operands of any length may begin on any arbitrary byte boundary.

For use in vector operations, a vector address generator is also provided. In parallel to the ASU and vector processing units, the ATU autonomously generates successive logical addresses of vector elements.

VECTOR PROCESSING SUBSYSTEM (VPS)

Both logically and physically integrated within the CPU is the vector processing subsystem (VPS), which consists of a vector control unit (VCU) and two vector processing units (VP0, VP1). The VPS incorporates many novel design features, including a static dataflow scheduling mechanism controlling a multi-pipe operand pipeline among multiple functional units. The multi-pipe pipeline uses two identical logic boards to process data simultaneously. This permits 64-bit operands to be processed every 100 nanoseconds and 32-bit operands to be processed every 50 nanoseconds. Further enhancing performance is the presence of three functional units; the first for add, subtract, and logical operations; the second for load, store, and vector edit; and the third for multiply and divide. Each functional unit is controlled by a separate 4096-word RAM-based microprogram control store. Each of these functional units is independently controlled and sequenced and can operate concurrently on 3 streams of independent data or be chained together to operate on one data stream. This structure provides a peak vector processing speed of 60 million operations per second. As a consequence of the static dataflow control, operations initiate as soon as their operands arrive at the designated functional unit. Since each functional unit contains an input operation queue, multiple instructions can be decoded and dispatched without their operands first being available.

To enhance the performance of vector processing, the VPS includes a set of high-speed vector accumulators. The vector accumulator set includes 8 independent registers, each capable of storing 128 elements, where each element may be up to 64 bits in width. These high-speed registers contribute to CONVEX's outstanding performance on both short and long vector problems.

Concurrently with vector processing, the ASU and IPU can perform operations on scalar operands, including conditional branches and fixed-point arithmetic. This "asymmetric parallel processing" results in maximum performance, since each functional unit is optimized for its specific task.

Enhancing the utility of the integrated vector processing subsystem is the provision for manipulation of 32-bit and 64-bit precision floating point operands and byte, halfword, 32-bit word, and 64-bit longword integers and logicals. A vector of indices is provided for high speed scatter/gather operations, and the inclusion of special-purpose registers such as Vector Length and Vector Stride allows processing of complex structures, including non-contiguous elements, which is difficult or impossible on other vector machines. A complete set of vector edit instructions permits compress/mask/merge operations to be executed concurrently with the ADD and MULTIPLY functional units. Other instructions are used to perform reductions on vectors to produce a scalar result.

PHYSICAL CACHE UNIT (PCU)

A physical cache is provided to accelerate both scalar and vector performance. The physical cache unit (PCU) has a capacity of 64 KBYTES organized as a 16384 by 36 bits, 50ns direct mapped data store. When the PCU requires a main memory word, the cache block referenced is loaded in a desired-word-first manner. To increase the overall performance, the PCU utilizes a write-back store strategy, so that main memory updates are performed only when needed.

When a vector load or store occurs, the PCU may either load the referenced vector into the data cache, or bypass the cache. If the cache is bypassed, sequential loads and stores of operands leave the previous contents of the cache unmodified. Data consistency during I/O operations is maintained by a separate set of tag stores in the memory control unit.

MAIN MEMORY EXPANSION TO 16 MWords

The CONVEX C-1 supports from one half to 16 MWords (128 MBytes) of directly addressable main memory. Memory modules (MAU's) may contain either one half MWords or 4 MWords of high-speed dynamic RAM. The system may contain up to 8 memory modules, and one half MWords and 4 MWords modules may be mixed in the same system.

Each MAU is organized as two banks of 4-way interleaved memory. Each bank is 72-bits wide, 64 for data and 8 for a single-bit correction, double-bit detection error code. Within each bank, either 1, 2, 3, or 4 memory words can be read or written in a sequential manner. After the first access, each additional access proceeds at 100 nanoseconds. In support of the physical cache, the memory bank can be accessed in a desired-word-first pattern; in other words, any block of 4 memory locations may be fetched using modulo-4 arithmetic, beginning with the location which is immediately required. This access method, as well as the ability to access individual words directly, optimally supports the different reference patterns from the CPU and I/O system.

The main memory system is dual-ported, with each port supporting 80 megabytes of bandwidth. One port is allocated to the CPU, while the other port is allocated to Input/Output.

SPECIFICATIONS FOR CONVEX C-1 COMPUTER SYSTEM

CENTRAL PROCESSING UNIT

HARDWARE SUPPORTED DATA TYPES: (SCALAR AND VECTOR, BYTE ADDRESSABLE) INTEGER *1, *2, *4, *8 LOGICAL *1, *2, *4, *8 REAL *4, *8 CHARACTER	
PROCESSOR CYCLE TIME: MAJOR: MINOR:	 100 nanoseconds 50 nanoseconds
MICROINSTRUCTION WORD SIZE: ASU	4096×80 (RAM)
MICROINSTRUCTION WORD SIZE: VPU FUNCTIONAL UNIT ADD/LOGICAL/SHIFT: MULT/DIVIDE: LOAD/STORE/COMPRESS/MERGE:	 4096×48 (RAM) 4096×48 (RAM) 4096×56 (RAM)
VIRTUAL ADDRESS SPACE:	4 Gigabytes
MAXIMUM USER PROGRAM:	2 Gigabytes
PAGE SIZE:	4096 Bytes
REFERENCED/MODIFIED BITS:	In Hardware, pair per pageframe
HARDWARE LOGIC FAMILY:	8000 Gate CMOS VLSI Gate Arrays, and high-speed advanced Schottky logic

MEMORY SYSTEM

MAXIMUM PHYSICAL MEMORY:	16 MWords (128 Megabytes)
I/O TO MAIN MEMORY BANDWIDTH:	80 megabytes/second
CPU TO MEMORY BANDWIDTH:	80 megabytes/second

INPUT/OUTPUT SYSTEM

I/O BANDWIDTH PER IOP:	8 megabytes/sec
MAXIMUM NUMBER OF IOP'S:	5
MULTIBUS CHASSIS PER IOP:	4
MULTIBUS BANDWIDTH:	4 megabytes/sec
ENVIRONMENTAL (Processor Cabinet Only)	
HARDWARE FORM FACTOR: CENTRAL PROCESSOR BOARD: MULTIBUS BOARD:	 19.3 inch×20 inch 6.75 inch×12 inch
POWER CONSUMED STANDARD: MAXIMUM:	 3200 Watts 4500 Watts
COOLING:	Forced air drawn from the front, exhausted to the rear.
AC POWER REQUIREMENTS:	208 VAC, 60Hz, 3 phase, 15 amps
OPERATING TEMPERATURE RANGE:	15–32 degrees centigrade.
VOLTAGE TOLERANCE:	184–264 VAC, phase to phase
FREQUENCY TOLERANCE:	47–63 Hz
CABINET SIZE (WITH INDUSTRIAL SKINS): WIDTH: HEIGHT: DEPTH:	 25.09 inches (19 inch RETMA rack) 62.5 inches 39.5 inches
CABINET WEIGHT:	500 pounds (estimated)
FCC COMPLIANCE:	Class A, Subpart J of Part 15.

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